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FINAL REPORT

TO

The Air Force Office of Scientific Research

on

Grant Number AFOSR-83-0315

from

J.C.Browne, Principal Investigator

The Department of Computer Science

The University of Texas at Austin

Austin, Texas 78712

17 December 1985

J.C.Browne

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1. List of Equipment Purchased

The funds provided by grant number AFOSR-83-0315 were combined with matching funds provided by the University of Texas to create a hardware and software development environment for parallel computer systems. The hardware development environment includes a chip and printed circuit board design and simulation capability and a high performance digital logic analyzer. The software development environment is a software-rich superminicomputer and a set of low-power graphics workstations. The total configuration includes a Digital Equipment Corporation VAX 11/750 computer system including the VMS operating system and a complement of other software, a Valid Logic computer-aided-design workstation including the Scald design system, a Tektronix DAS9129 high performance digital logic analyzer and a set of Apple Macintosh microcomputers to be used for terminals and as low-powered workstations. The fabrication of and the selections for the printed circuit boards for the four-processor nine-memory configuration of the Texas Reconfigurable Array Computer (TRAC) were also funded from this grant.

There was one change between the equipment complement proposed and that actually purchased. The functions of the hardware documentation system specified in the proposal were subsumed in the capabilities of the Valid Logic design system purchased with matching funds from the University of Texas. It was only necessary to make small additions to the Valid system to attain the specified documentation capabilities. This modification was approved by AFOSR on August 4, 1984.

The complete list of equipment purchased with the funds provided under grant number AFOSR is listed following.

1.1. VAX 11/750 Computer System — 95,619.95

- 750XA-AE Processor and Memory
- RAU81-CA Disk and Controller
- TU80-AA Magnetic Tape System

- DMF32-LP Multiplexer
- LA120-DA Console Printer
- QD126-DZ Pascal
- QD100-DZ Fortran
- QD001-HM VMS
- QD100-HG Fortran Update
- QD126-HG Pascal Update
- A462 Line Printer
- DEUNA-AA Ethernet System
- VMZ-32N Port Expander

1.2. Logic Analyzer-Tektronix **27,003.67**

- DAS9129 Modular Digital
- Analysis System

1.3. Custom PC Boards For TRAC **8780.38**

- Fabrication
- Memory Chips
- Miscellaneous Parts (Cables, etc.)

1.4. Documentation System **4864.00**

PIB Board for Valid Workstation Graphics Codes for Visual Terminal

TOTAL **$149,960.00**

2. Research Projects Utilizing This Equipment

The principal research projects supported by the equipment purchased with the funds supplied by this grant were the AFOSR projects "High Performance Parallel Computing" (AFOSR Grant Number F49620-83-C-0049 and F49620-84-C-0020). It has also been used by other Department of Defense sponsored research projects. It has also been important for research in parallel computing sponsored by the Department of Energy under Grant DE-ASO5-81ER10987 and the National Science Foundation under Grant Number DCR-8116099 (formerly MCS-8116099). The paragraphs which follow define and describe the use in research of the equipment purchased under this grant and the matching grant from the University of Texas.

2.1. Parallel Computing on TRAC and Other

The two major uses of the equipment have been design, documentation, and validation of printed circuit boards for TRAC and/or a development environment for parallel software systems including the operating system for TRAC, the Computation Structures Language (CSL) [BRO82] and the Task Level Data Flow Language (TDFL). The VAX 11/750 has also served as the front-end and back-end coupling TRAC to the outside world including serving as the host system for the TRAC Macro-Assembler. The instruction level simulator for TRAC which was originally developed for the DEC 2060 will be migrated to the TRAC VAX.

The Valid Logic workstation and the VAX combine to make a design environment which has been used for the design of several printed circuit boards for TRAC. The boards which have been designed using this facility include the memory boards now being used in TRAC and a board which interfaces a floating point unit to the TRAC processor. The Valid workstation has also been used to create documentation of other printed circuit boards already in use in TRAC.

The Tektronix logic analyzer has been the critical factor in the dramatic improvement of hardware stability of TRAC which was obtained in 1983/84. It has given an order of magnitude enhancement in the ability of the technical staff to diagnose and

correct hardware faults.

The VAX 11/750 has been the host system for the TRAC Macro-Assembler. The Macro-Assembler has been the principal vehicle for development of programs for testing of TRAC and for the development of the applications which have been coded. Assembly language programs are written and assembled on the VAX and then down-line loaded to TRAC through an RS232 port treating TRAC as a terminal. The instruction level simulator for TRAC is being ported to the VAX 11/750. Further studies of the TRAC operating system will be conducted in this environment.

The VAX 11/750 has also been used as the host for part of the development of the CSL and TDFL parallel programming languages mentioned preceding. TRAC itself has not reached a state of sufficient stability to directly serve as a host for execution of parallel programs written in these languages. Development of the run-time systems and translators for these systems have been partially hosted on the VAX but are executed on the dual processor Control Data Corporation Cyber 170/750 configuration at the Computation Center of the University of Texas. The Master's degree thesis of R. O'Dell [ODE85] describes the design of the CSL run-time system.

2.2. Simulation Models of Distributed Systems

The University of Texas was a sub-contractor to Honeywell for Rome Air Defense Center contract number F30602-82-C-0154. The research executed under this contract required extensive simulations of the execution of distributed systems. These simulations, which included consideration of occurrence of faults in the host processors of the distributed systems, were executed on this VAX 11/750. The results of these simulations have appeared in two papers [FER84] and [PAL85].

3. References

[BRO82] Browne, J.C., *et al*, "A Language for Specification and Programming of Reconfigurable Parallel Computation Structures," Proc 1982 ICPP, Bellaire, Mich., Aug.1980, pp 142-151

[FER84] Fernandes, V., *et al*, "Some Performance Models of Distributed

Systems," Proc. XV Intl.Conf on Man. and Performance Evaluation of Computer Systems, San Francisco, Dec.1985, pp 30-37

[PAL85] Palmer, A., *et al*, "A Performance Model of a Fault-Tolerant Distributed System for Evaluation of Reliability Mechanisms," Proc. XVI, Intl. Conf on Man. and Perf. of Computer Systems, Dallas, Dec.1985

[ODE85] O'Dell, R., "On The Parallel Structuring Of Resource Management," Master's Thesis, Dept. of Computer Sciences, University of Texas at Austin, Nov. 1985